What is claimed is:

1. An EER amplifier for amplifying a signal, comprising:

(I) a divider for dividing said signal into a phase signal and an envelope signal;

(II) a first RF amplifier for amplifying said signal, said first amplifier having a bias supply input;

(III) an EER modulator having input receiving said envelope signal and an output coupled to said bias supply input of said first RF amplifier, said EER modulator comprising:

(A) a high frequency power operational amplifier for amplifying a high frequency portion of said envelope signal, and having an output coupled to said output of said EER modulator;

(B) a high efficiency power amplifier for amplifying a remaining portion of said envelope signal, said power amplifier having:

(1) a current control input,

(2) a current monitoring output,

(3) a power output coupled to said output of said EER modulator;

(C) a feedback control loop comprising:

(1) a current-to-voltage conversion amplifier having an input coupled to said current monitoring output of said high efficiency power amplifier and an output,

(2) an input buffer amplifier having an input coupled to receive said envelope signal and an output;

(3) a summing amplifier having:

(a) an input coupled to the outputs of: (a) said current-to-voltage conversion amplifier and (b) said input buffer amplifier, and

(b) an output coupled to said current control input of said high efficiency power amplifier.

2. The apparatus of Claim 1 wherein said power amplifier has a first gain and said feedback control loop has a second gain, and wherein the product of said first and second gains provides an active resistance at the power output of said high efficiency power amplifier exceeding an output impedance of said high frequency operational power amplifier.

3. The apparatus of Claim 2 wherein said high frequency operational power amplifier has an output impedance less than 1 Ohm, and wherein said active resistance of said power amplifier is between about 5 and 10 Ohms.

4. The apparatus of Claim 3 wherein said active resistance is between about 1 and 10 Ohms.

5. The apparatus of Claim 1 wherein high efficiency power amplifier comprises a pair of power output transistors having source-to-drain channels connected in series, said power output being the connection between said pair of output transistors, said current monitoring output comprising a drain of one of said pair of transistors, said apparatus further comprising a voltage drop resistor connected to said drain, said input of said current-to-voltage converter amplifier being connected across said voltage drop resistor.

6. The apparatus of Claim 1 wherein said high efficiency power amplifier is a switching pulse-width modulation amplifier comprising:

a pulse-width modulation controller for generating a complementary pair of pulse signals whose pulse widths are functions of said current control input;

a pair of power FETs having source-to-drain channels connected in series across a bias power source and respective gates controlled by respective ones of said complementary pair of pulse signals, said source-to-drain channels being connected together at a node constituting said power output of said power amplifier.

7. The apparatus of Claim 6 further comprising respective preamplifier stages for amplifying respective ones of said complementary pair of pulse signals.

8. The apparatus of Claim 6 wherein said pulse-width modulation controller comprises a voltage to pulse width generator and a complementary pair of outputs transitioning between opposite binary states upon a change in amplitude comparison between the output of said summing amplifier and the pulse width generator.

9. An amplifier comprising:

a divider circuit for dividing an incoming signal into a low frequency amplitude modulation envelope signal and a phase portion;

a first RF amplifier for amplifying said phase portion, said first RF amplifier having a bias supply input;

a modulator connected to receive said envelope signal for furnishing a modulated bias supply to said bias supply input of said first RF amplifier, said modulator comprising:

a high frequency operational amplifier for amplifying a higher frequency portion of said envelope signal and a power amplifier for amplifying a lower frequency portion of said envelope signal, said power amplifier having an output current control input and an output current monitoring port;

a feedback control loop having first and second inputs and a control output connected to said output current control input of said power amplifier, said first and second inputs connected respectively to said envelope signal and said output current monitoring port of said power amplifier, said feedback control loop comprising means for producing at said control output a signal which is a function of a difference between said envelope signal and the output current of said power amplifier, whereby said feedback control loop

controls the output current of said power amplifier so as to minimize said difference.

10. The amplifier of Claim 9 wherein said power amplifier has a first gain and said feedback control loop has a second gain, the combination of said power amplifier and said feedback control loop having an active output resistance which is a function of the product
of said first and second gains.

11. The amplifier of Claim 10 wherein said high frequency operational amplifier has a low output impedance and said active output resistance of said power amplifier is greater than said low output impedance of said high frequency operational amplifier by less than two orders of magnitude.

12. The amplifier of Claim 11 wherein said active output resistance is greater than said low output impedance by less than one order of magnitude.

13. The amplifier of Claim 12 wherein said active output resistance is between about 1 and 10 Ohms.

14. The amplifier of Claim 9 wherein said power amplifier is a pulse-width modulated amplifier having a large output current capability at low frequencies.

15. The amplifier of Claim 14 wherein said power amplifier comprises an output node connected by a pair of transistors to respective opposing voltage sources and a pulse-width modulation controller responsive to said output current control input, for applying complementary pulse-width modulated signals to gates of respective ones of said pair of transistors.